

Suppression of Forward-Bias Degradation in 3.3 kV DMOSFETs

We-P-02

Fabricated on 4H-SiC Bonded Substrates

*Seiji Ishikawa¹, Yuta Higashi², Motoki Kobayashi³, Mitsuo Okamoto¹, Kazutoshi Kojima¹, Shinsuke Harada¹

1. Advanced Power Electronics Research Center, National Institute of Advanced Industrial Science and Tech. (Japan),

2. PHENITEC Semiconductor Corp. (Japan), 3. Sumitomo Metal Mining Co., Ltd. (Japan)

Objective

Our research has focused on SiC bonded substrates.

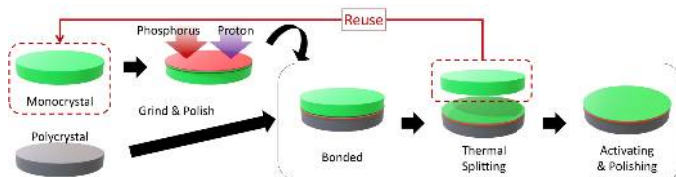
- Reduction of on-state resistance in 1.2 kV DMOSFETs [1]
- Suppression of switching loss in body diodes [1]
- Reduction of forward-bias degradation in 1.2 kV DMOSFETs and PIN diodes [1-2]

In 3.3 kV devices, drift resistance dominates the total on-resistance, limiting the benefit of bonded substrates.

This work explores whether bonded substrates provide advantages beyond on-resistance reduction, particularly in body-diode performance and forward-bias degradation.

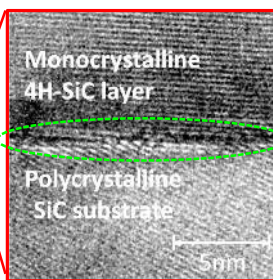
What is a Bonded substrate?

A structure in which an extremely thin (<1 μm) 4H-SiC single-crystal layer is bonded to an n-type, low-resistance polycrystalline 3C-SiC substrate by surface-activated bonding.



Thickness < 1 μm

4H-SiC (Transfer layer)
Direct bonding
poly-SiC (3C-SiC)
 $\rho < 10 \text{ m}\Omega\text{cm}$



Cross-sectional TEM

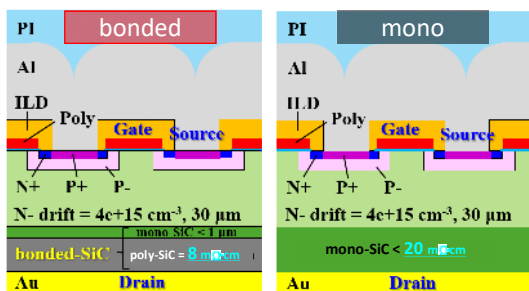
Experiments

3.3 kV DMOSFET fabrication

- 3.3 kV DMOSFETs were fabricated on both a 4H-SiC single-crystalline substrate (mono) and a bonded substrate (bonded).

Measurement and characterization

- Static characteristics
- Reverse-recovery characteristics of the body diode
- Forward-current stress testing



Results

Static characteristics of 3.3 kV-DMOSFET

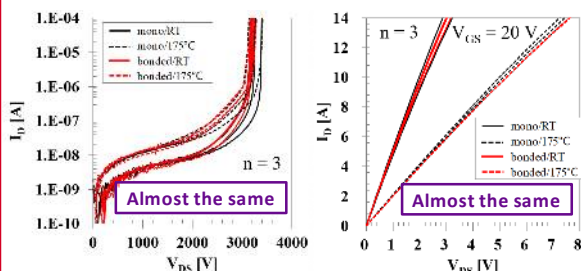


Fig. 2 Blocking characteristics

Fig. 3 I_D - V_{DS} characteristics

The I_D - V_D characteristics were almost the same.

This is because the drift resistance, which is needed to maintain the high breakdown voltage of 3.3 kV, dominates the total on-resistance.

Therefore, the benefit of the low-resistance substrate in the bonded structure was limited.

Forward-current stress testing & PL imaging results after the test

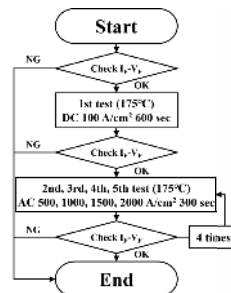


Fig. 7 Flowchart of the forward-current stress test

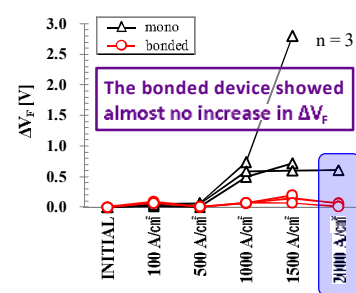


Fig. 8 ΔV_F of the body diode after forward testing

Static and dynamic characteristics of body-diode

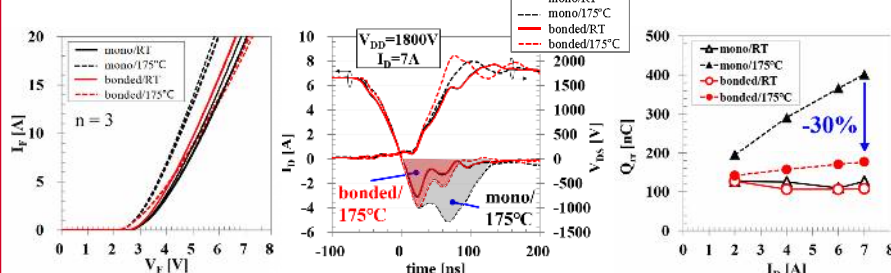


Fig. 4 Temperature dependence of I_F - V_F characteristics

Fig. 5 Reverse recovery waveforms of the body diode

Fig. 6 Temperature dependence of Q_{rr} - I_D characteristics

V_F increased with temperature in the bonded device.

At 175 °C, Q_{rr} was 30% lower for the bonded device than for the mono device.

These results are consistent with previously reported findings that hydrogen ion implantation shortens the carrier lifetime in bonded devices. [3-6]

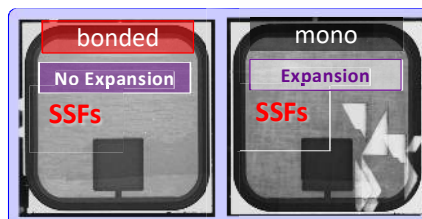


Fig. 9 PL imaging results after 2000 A/cm² forward-current stress (using a 420 nm band-pass filter)

These results are similar to those of 1.2 kV-class devices on bonded substrates. [1-2]

Discussion

The bonded device exhibited reduced Q_{rr} and suppressed SSF expansion, suggesting lower minority carrier density in the drift layer.

The 3.3 kV-class device showed behavior similar to previous bonded-substrate studies [1-6], which may be attributable to trap-induced lifetime reduction in the bonded substrate.

Further research is needed to elucidate this mechanism.

Conclusion

3.3 kV DMOSFETs fabricated on bonded substrates showed:

- Breakdown voltage and on-resistance were almost the same as those of the mono device.
- 30% reduction in body-diode recovery loss at 175 °C.
- High tolerance to high forward-current stress.

The bonded substrate showed improved body-diode behavior, including reduced Q_{rr} and suppressed SSF expansion.

These results suggest that a lower minority carrier density may contribute to the improved degradation tolerance of bonded substrate 3.3 kV DMOSFETs.

References

- [1] Y. Higashi et al., *Proc. ICSCRM*, 2024, p. 541.
- [2] N. Hatta et al., *Key Engineering Materials*, Vol. 948, pp. 107–113, 2023.
- [3] H. Uchida et al., *Defect and Diffusion Forum*, Vol. 434, pp. 39–44, 2024.
- [4] M. Alaluss et al., *Key Engineering Materials*, Vol. 1024, pp. 49–56, 2025.
- [5] H. Uchida et al., *Solid State Phenomena*, Vol. 375, pp. 21–27, 2025.
- [6] M. Alaluss et al., *Proc. ISPSD*, 2025.

Acknowledgement

This study was carried out under a joint research project of Tsukuba Power Electronics Constellations (TPEC). S. Ishikawa is assigned from PHENITEC Semiconductor Corp.